

8. (Amended) The circuit substrate according to claim 1, wherein a surface irregularity is formed at a bonding site between said conductor and said wiring layers.

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9. (Amended) A circuit substrate comprising:
an insulating base; and
a conductor provided inside said insulating base to electrically connect an interlayer of said insulating base,
wherein a tensile strength of said conductor in a base thickness direction is greater than a bonding strength between said conductor and said insulating base on a wall surface of said conductor.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended the specification to address the objection to the drawings. Specifically, the specification has been amended to expressly refer to copper foil 1g' illustrated in Fig. 12D. In addition, the title of the invention has been amended to more precisely identify the subject matter of the invention. With regard to the objection to the specification due to the use of the term "prepreg", Applicants wish to inform the Examiner that the term is clearly defined, for example, on page 9 of the specification.

With regard to the claims, claim 8 has been amended to address the rejection thereof under 35 U.S.C. § 112, second paragraph, and claims 1-3 and 5-9 have been amended to clarify the intended subject matter of the present invention. It is noted that the amendments to the claims are not intended to further limit the scope of the originally filed claims, but only clarify the claimed invention. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that the pending claims are patentable over the cited prior art references.

II. The Rejection Of Claim 8 Under 35 U.S.C. § 112, Second Paragraph

Claim 8 was rejected under 35 U.S.C. § 112, second paragraph, for being indefinite on the basis that the meaning of the term "irregularity" as utilized in the claim was unclear. In response, Applicants have amended claim 8 so as to recite that a "surface irregularity" is formed at the bonding site between the conductor and wiring layers. As shown in Fig. 13, surface irregularities 7b are introduced in order to enhance the bonding strength between the wiring and the conductive paste (see, pages 31 and 32 of the specification). It is respectfully submitted that, as amended, claim 8 satisfies all requirements of 35 U.S.C. § 112, second paragraph.

III. The Rejection Of The Claims Under 35 U.S.C. § 103

Claims 1-9 were rejected under 35 U.S.C. § 103 as being unpatentable over

USP No. 6,010,769 to Sasoka. For the following reasons, Applicants respectfully submit that the pending claims are patentable over Sasaoka.

As recited by claims 1 and 9, the present invention relates to a circuit substrate having multiple wiring layers separated by an insulating layer, which have vias formed therein, which are filled with conductive paste (i.e., conductor) in order to couple the wiring layers to one another. Importantly, the bonding strength between the wiring layer and the conductor is greater than the bonding strength between the wiring layer and the insulating layer. As a result, as explained in detail in the specification (e.g., see, pages 16 and 17), because of the foregoing relationship in bonding strength, when stress is caused by the difference in thermal expansion coefficients between the insulating layer and the conductive paste, the interface between the wiring layer and the insulating layer serves to absorb the stress, thereby reducing the possibility of a disconnect between the conductive paste and the wiring layer.

Turning to the cited prior art and the pending rejection, it is admitted in the pending rejection that Sasaoka fails to disclose or suggest the limitation regarding the bonding strength between the wiring layer and the conductor being greater than the bonding strength between the wiring layer and the insulating layer. The pending rejection asserts that the foregoing limitation, as recited in the original claims, was merely a "product by process" limitation and therefore not provided any patentable weight.

Applicants respectfully disagree that the foregoing limitation as recited by the original claims was a "product by process" limitation. However, in an effort to expedite prosecution of the application, the Applicants have amended claims 1 and 9 so as to make clear that the foregoing limitation is a structural element. As recited by amended claim 1 and 9, it is clear that the ***structure of the circuit substrate*** must be such that the bonding strength between the wiring layer and the conductor is greater than the bonding strength between the wiring layer and the insulating layer. Clearly, the foregoing element cannot be deemed a "process" limitation, as the limitation is silent regarding how the structure is formed. Thus, it is respectfully submitted that the limitation must be afforded weight as a structural element of the claims.

Accordingly, as each and every limitation of the claimed invention must be either disclosed or suggested by the cited prior art reference in order to establish a *prima facie* case of obviousness, (see, M.P.E.P. § 2143.03), and it has been admitted that Sasaoka fails to do so, it is respectfully submitted that claims 1 and 9, and the claims dependent thereon, are patentable over Sasoka.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the

independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987).

Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.


V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

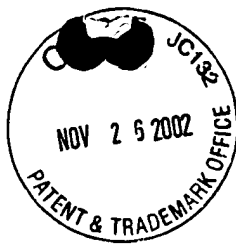
If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

The title of the invention has been amended as follows:

A CIRCUIT SUBSTRATE HAVING IMPROVED CONNECTION RELIABILITY
AND A METHOD FOR MANUFACTURING [METHOD THEREOF] THE SAME

IN THE SPECIFICATION:

Paragraph beginning at page 30, line 3, has been amended as follows:

Next, as shown in Fig. 12D, a copper foil 1g (and 1g') is laminated and placed on both surfaces of the prepreg base 1a'. Then, the prepreg base 1a' and the copper foil 1g (and 1g') are heated while being compressed along the thickness direction of the prepreg base 1a'. This integrates the prepreg base 1a' with the copper foil 1g (and 1g'), and forms a bond between the copper foil 1g (and 1g') and the conductive paste 1d' to establish an electrical connection.

IN THE CLAIMS:

Please amend claims 1, 2, 3 and 5-9 as follows:

1. (Amended) A circuit substrate comprising:

an insulating base;

wiring layers provided disposed on said insulating base; and

a conductor provided disposed inside said insulating base to electrically connect

between said wiring layers in an interlayer of said insulating base,

wherein a bonding strength between said wiring layers and said conductor is [compared with] greater than a bonding strength between said wiring layers and said insulating base [to be relatively lowered the latter].

2. (Amended) The circuit substrate according to claim 1, wherein said conductor contains a resin composition, and [a relative relationship of said bonding strength is established by comparing] a glass transition temperature of the resin composition [with] is set lower than a glass transition temperature of a resin composition constituting a surface site of said insulating base [to set the latter higher].

3. (Amended) The circuit substrate according to claim 1, wherein said insulating base and said conductor contain a thermosetting epoxy resin composition, and [the relative relationship of said bonding strength is established by comparing] a volume content of the thermosetting epoxy resin in said conductor is set larger than [with] a volume content of the thermosetting epoxy resin in said insulating base [to set the latter lower].

5. (Amended) The circuit substrate according to claim 1, wherein [the relative relationship of said bonding strength is established by forming] a metal cohesion is

applied between said conductor and said wiring layers.

6. (Amended) The circuit substrate according to claim 1, wherein [the relative relationship of said bonding strength is established by providing] a non-bonding region is provided at a part of a bonding site between said wiring layers and said insulating base in the adjacency of said conductor.

7. (Amended) The circuit substrate according to claim 1, wherein [the relative relationship of said bonding strength is established by providing] a region containing an uncured resin component is provided at a bonding site between said wiring layers and said insulating base in the adjacency of said conductor.

8. (Amended) The circuit substrate according to claim 1, wherein [the relative relationship of said bonding strength is established by forming an] a surface irregularity is formed at a bonding site between said conductor and said wiring layers.

9. (Amended) A circuit substrate comprising:
an insulating base; and
a conductor provided inside said insulating base to electrically connect an interlayer of said insulating base,

wherein a tensile strength of said conductor in a base thickness direction is
[compared with] greater than a bonding strength between said conductor and said
insulating base on a wall surface of said conductor [to set the latter relatively lower].